Chapter 6  Physics of MOS Transistors

- 6.1 Structure of MOSFET
- 6.2 Operation of MOSFET
- 6.3 MOS Device Models
- 6.4 PMOS Transistor
- 6.5 CMOS Technology
- 6.6 Comparison of Bipolar and CMOS Devices

Chapter Outline

Operation of MOSFETs
- MOS Structure
- Operation in Triode Region
- Operation in Saturation
- I/V Characteristics

MOS Device Models
- Large-Signal Model
- Small-Signal Model

PMOS Devices
- Structure
- Models
Metal-Oxide-Semiconductor (MOS) Capacitor

The MOS structure can be thought of as a parallel-plate capacitor, with the top plate being the positive plate, oxide being the dielectric, and Si substrate being the negative plate. (We are assuming P-substrate.)

Structure and Symbol of MOSFET

This device is symmetric, so either of the n+ regions can be source or drain.
**State of the Art MOSFET Structure**

- The gate is formed by polysilicon, and the insulator by Silicon dioxide.

**Formation of Channel**

- First, the holes are repelled by the positive gate voltage, leaving behind negative ions and forming a depletion region. Next, electrons are attracted to the interface, creating a channel ("inversion layer").
The inversion channel of a MOSFET can be seen as a resistor. Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.

As the gate voltage decreases, the output drops because the channel resistance increases. This type of gain control finds application in cell phones to avoid saturation near base stations.
The MOS characteristics are measured by varying $V_G$ while keeping $V_D$ constant, and varying $V_D$ while keeping $V_G$ constant.

(d) shows the voltage dependence of channel resistance.

Small gate length and oxide thickness yield low channel resistance, which will increase the drain current.
Effect of W

- As the gate width increases, the current increases due to a decrease in resistance. However, gate capacitance also increases thus, limiting the speed of the circuit.
- An increase in W can be seen as two devices in parallel.

Channel Potential Variation

- Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.
Channel Pinch-Off

- As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain.
- When $V_D - V_G = V_{th}$, the channel at drain totally pinches off, and when $V_D - V_G > V_{th}$, the channel length starts to decrease.

Channel Charge Density

- The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.

$$Q = WC_{ox} (V_{GS} - V_{TH})$$

- The channel charge density is equal to the gate capacitance times the gate voltage in excess of the threshold voltage.
Charge Density at a Point

Let \( x \) be a point along the channel from source to drain, and \( V(x) \) its potential; the expression above gives the charge density (per unit length).

\[
Q(x) = WC_{ox} [V_{GS} - V(x) - V_{TH}]
\]

Charge Density and Current

The current that flows from source to drain (electrons) is related to the charge density in the channel by the charge velocity.

\[
I = Q \cdot v
\]
Drain Current

\[ v = +\mu_n \frac{dV}{dx} \]

\[ I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx} \]

\[ I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \]

Parabolic \( I_D - V_{DS} \) Relationship

- By keeping \( V_G \) constant and varying \( V_{DS} \), we obtain a parabolic relationship.
- The maximum current occurs when \( V_{DS} \) equals to \( V_{GS} - V_{TH} \).
**I_D-V_DS for Different Values of V_GS**

\[ I_{D,\text{max}} \propto (V_{GS} - V_{TH})^2 \]

- **Linear Resistance**
  - At small V_{DS}, the transistor can be viewed as a resistor, with the resistance depending on the gate voltage.
  - It finds application as an electronic switch.

\[
R_{on} = \frac{1}{\mu_{n}C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}
\]
Application of Electronic Switches

- In a cordless telephone system in which a single antenna is used for both transmission and reception, a switch is used to connect either the receiver or transmitter to the antenna.

Effects of On-Resistance

- To minimize signal attenuation, $R_{on}$ of the switch has to be as small as possible. This means larger $W/L$ aspect ratio and greater $V_{GS}$.

CH 6  Physics of MOS Transistors
**How to Determine ‘Region of Operation’**

- When the potential difference between gate and drain is greater than $V_{TH}$, the MOSFET is in triode region.
- When the potential difference between gate and drain becomes equal to or less than $V_{TH}$, the MOSFET enters saturation region.
When the region of operation is not known, a region is assumed (with an intelligent guess). Then, the final answer is checked against the assumption.

Channel-Length Modulation

The original observation that the current is constant in the saturation region is not quite correct. The end point of the channel actually moves toward the source as \( V_D \) increases, increasing \( I_D \). Therefore, the current in the saturation region is a weak function of the drain voltage.
Unlike the Early voltage in BJT, the channel-length modulation factor can be controlled by the circuit designer. For long L, the channel-length modulation effect is less than that of short L.

Transconductance

<table>
<thead>
<tr>
<th>$\frac{W}{L}$ Constant</th>
<th>$\frac{W}{L}$ Variable</th>
<th>$\frac{W}{L}$ Variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS} - V_{TH}$ Variable</td>
<td>$V_{GS} - V_{TH}$ Constant</td>
<td>$V_{GS} - V_{TH}$ Constant</td>
</tr>
<tr>
<td>$g_m \propto \sqrt{I_D}$</td>
<td>$g_m \propto I_D$</td>
<td>$g_m \propto \sqrt{\frac{W}{L}}$</td>
</tr>
<tr>
<td>$g_m \propto V_{GS} - V_{TH}$</td>
<td>$g_m \propto \frac{W}{L}$</td>
<td>$g_m \propto \frac{1}{V_{GS} - V_{TH}}$</td>
</tr>
</tbody>
</table>

$g_m = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})$

$g_m = \frac{2}{V_{GS} - V_{TH}} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D$

$g_m = \frac{2}{V_{GS} - V_{TH}} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D$

Transconductance is a measure of how strong the drain current changes when the gate voltage changes.

It has three different expressions.
Doubling of $g_m$ Due to Doubling W/L

- If W/L is doubled, effectively two equivalent transistors are added in parallel, thus doubling the current (if $V_{GS} - V_{TH}$ is constant) and hence $g_m$.

Velocity Saturation

- Since the channel is very short, it does not take a very large drain voltage to velocity saturate the charge particles.
- In velocity saturation, the drain current becomes a linear function of gate voltage, and $g_m$ becomes a function of $W$. 

$$I_D = V_{sat} \cdot Q = V_{sat} \cdot W C_{ox} (V_{GS} - V_{TH})$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = V_{sat} W C_{ox}$$
**Body Effect**

As the source potential departs from the bulk potential, the threshold voltage changes.

\[ V_{TH} = V_{TH0} + \rho \left( \sqrt{2}\phi_F + V_{SB} - \sqrt{2}\phi_F \right) \]

---

**Large-Signal Models**

- Based on the value of \( V_{DS} \), MOSFET can be represented with different large-signal models.

- **(a)**
  \[ V_{GS} > V_{TH} \]
  \[ V_{DS} > V_{GS} - V_{TH} \]
  \[ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{GS}) \]

- **(b)**
  \[ V_{GS} > V_{TH} \]
  \[ V_{DS} < V_{GS} - V_{TH} \]
  \[ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} + V_{DS}^2] \]

- **(c)**
  \[ V_{GS} > V_{TH} \]
  \[ V_{DS} < 2(V_{GS} - V_{TH}) \]
  \[ R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \]
**Example: Behavior of $I_D$ with $V_1$ as a Function**

Since $V_1$ is connected at the source, as it increases, the current drops.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_T - V_1)^2$$

**Small-Signal Model**

- When the bias point is not perturbed significantly, small-signal model can be used to facilitate calculations.
- To represent channel-length modulation, an output resistance is inserted into the model.

$$r_o \approx \frac{1}{\lambda I_D}$$
PMOS Transistor

Just like the PNP transistor in bipolar technology, it is possible to create a MOS device where holes are the dominant carriers. It is called the PMOS transistor.

It behaves like an NMOS device with all the polarities reversed.

PMOS Equations

- \( I_{D,\text{sat}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 - \lambda V_{DS}) \)
- \( I_{D,\text{pri}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \left[ 2(V_{GS} - V_{TH}) V_{DS}^2 - V_{DS}^3 \right] \)
- \( I_{D,\text{sat}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \left( |V_{GS}| - |V_{TH}| \right)^2 (1 + \lambda |V_{DS}|) \)
- \( I_{D,\text{pri}} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \left[ 2(|V_{GS}| - |V_{TH}|) |V_{DS}| - V_{DS}^2 \right] \)
Small-Signal Model of PMOS Device

- The small-signal model of PMOS device is identical to that of NMOS transistor; therefore, $R_X$ equals $R_Y$ and hence $(1/gm)||r_o$.

CMOS Technology

- It is possible to grow an n-well inside a p-substrate to create a technology where both NMOS and PMOS can coexist.
- It is known as CMOS, or “Complementary MOS”.

CH 6  Physics of MOS Transistors
Comparison of Bipolar and MOS Transistors

<table>
<thead>
<tr>
<th>Bipolar Transistor</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exponential Characteristic</td>
<td></td>
</tr>
<tr>
<td>Active: $V_{CB} &gt; 0$</td>
<td>Quadratic Characteristic</td>
</tr>
<tr>
<td>Saturation: $V_{CB} &lt; 0$</td>
<td>Saturation: $V_{DS} &gt; V_{GS} - V_{TH}$</td>
</tr>
<tr>
<td>Finite Base Current</td>
<td>Triode: $V_{DS} &lt; V_{GS} - V_{TH}$</td>
</tr>
<tr>
<td>Early Effect</td>
<td>Zero Gate Current</td>
</tr>
<tr>
<td>Diffusion Current</td>
<td>Channel-Length Modulation</td>
</tr>
<tr>
<td>-</td>
<td>Drift Current</td>
</tr>
<tr>
<td></td>
<td>Voltage-Dependent Resistor</td>
</tr>
</tbody>
</table>

- Bipolar devices have a higher $g_m$ than MOSFETs for a given bias current due to its exponential IV characteristics.

Chapter 7 CMOS Amplifiers

- 7.1 General Considerations
- 7.2 Common-Source Stage
- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples
Chapter Outline

General Concepts
- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers
- Common-Source Stage
- Common-Gate Stage
- Source Follower

MOS Biasing

Voltage at X is determined by $V_{DD}$, $R_1$, and $R_2$.

$V_{GS} = -V_1 - V_{th} + \sqrt{V_1^2 + 2V_1 \left( \frac{R_2 V_{DD}}{R_1 + R_2} - V_{th} \right)}$

$V_1 = \frac{1}{\mu_C \frac{W}{L} R_S}$

$V_{GS}$ can be found using the equation above, and $I_D$ can be found by using the NMOS current equation.
The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across $R_G$.

$I_D R_D + V_{GS} + R_S I_D = V_{DD}$

When in saturation region, a MOSFET behaves as a current source.

- NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from $V_{DD}$ to a point (sources current).
CH7 CMOS Amplifiers

Common-Source Stage

\[ \lambda = 0 \]
\[ A_v = -g_m R_D \]
\[ A_v = -\sqrt{2\mu_C C_{ox} \frac{W}{L} I_D R_D} \]

Operation in Saturation

\[ R_D I_D < V_{DD} - (V_{GS} - V_{TH}) \]

- In order to maintain operation in saturation, \( V_{out} \) cannot fall below \( V_{in} \) by more than one threshold voltage.
- The condition above ensures operation in saturation.
CS Stage with $\lambda=0$

\[ A_v = -g_m R_L \]
\[ R_{in} = \infty \]
\[ R_{out} = R_L \]

However, Early effect and channel length modulation affect CE and CS stages in a similar manner.
CS Gain Variation with Channel Length

Since $\lambda$ is inversely proportional to $L$, the voltage gain actually becomes proportional to the square root of $L$.

\[
|A_v| = \sqrt{\frac{2\mu_n C_{ox} W}{L}} \lambda \sqrt{I_D} \propto \frac{2\mu_n C_{ox} W L}{I_D}
\]

CS Stage with Current-Source Load

To alleviate the headroom problem, an active current-source load is used. This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.
PMOS CS Stage with NMOS as Load

\[ A_v = -g_{m2} \left( r_{\Omega_1} \parallel r_{\Omega_2} \right) \]

- Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.

CS Stage with Diode-Connected Load

\[ A_v = -g_{ml} \cdot \frac{1}{g_{m2}} = -\frac{(W/L)_1}{(W/L)_2} \]
\[ A_v = -g_{ml} \left( \frac{1}{g_{m2}} \parallel r_{\Omega_2} \parallel r_{\Omega_1} \right) \]

- Lower gain, but less dependent on process parameters.
CS Stage with Diode-Connected PMOS Device

- Note that PMOS circuit symbol is usually drawn with the source on top of the drain.

\[ A_v = -g_{m2} \left( \frac{1}{g_{m1} || r_{o1} || r_{o2}} \right) \]

CS Stage with Degeneration

- Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.

\[ A_i = \frac{R_D}{1 + g_m R_S} \]

\[ \lambda = 0 \]
Example of CS Stage with Degeneration

A diode-connected device degenerates a CS stage.

\[ A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \]

CS Stage with Gate Resistance

Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.
Similar to the bipolar counterpart, degeneration boosts output impedance.

\[ r_{out} \approx g_m r_o R_S + r_O \]

Output Impedance Example (I)

When \(1/g_m\) is parallel with \(r_{o2}\), we often just consider \(1/g_m\).
Output Impedance Example (II)

In this example, the impedance that degenerates the CS stage is $r_O$, instead of $1/g_m$ in the previous example.

$R_{out} \approx g_m r_O (r_O + r_O)$

CS Core with Biasing

Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.
Common-Gate Stage

- Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.

\[ A_v = g_m R_D \]

Signal Levels in CG Stage

- In order to maintain M1 in saturation, the signal swing at \( V_{out} \) cannot fall below \( V_b - V_{TH} \).
The input and output impedances of CG stage are similar to those of CB stage.

When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.
Generalized CG Behavior

- When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).
- The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

\[ R_{out} = (1 + g_m r_O) R_s + r_O \]

Example of CG Stage

- Diode-connected \( M_2 \) acts as a resistor to provide the bias current.

\[ \frac{v_{out}}{v_{in}} = \frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_s} \]
\[ R_{out} \approx g_m r_{o1} \left( \frac{1}{g_m} + R_s \right) + r_{o1} \left\| R_D \right\| \]
CG Stage with Biasing

- $R_1$ and $R_2$ provide gate bias voltage, and $R_3$ provides a path for DC bias current of $M_1$ to flow to ground.

$$v_{out} = \frac{R_3}{R_3 || \left(1/g_m\right)} \cdot g_m R_D$$

Source Follower Stage

- $A_v < 1$

Input Applied to Gate

Output Sensed at Source
Similar to the emitter follower, the source follower can be analyzed as a resistor divider.

\[
\begin{align*}
V_{out} &= r_o || R_L \\
V_{in} &= \frac{1}{g_m} + r_o || R_L
\end{align*}
\]

In this example, \( M_2 \) acts as a current source.
Output Resistance of Source Follower

The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.

Source Follower with Biasing

- $R_G$ sets the gate voltage to $V_{DD}$, whereas $R_S$ sets the drain current.
- The quadratic equation above can be solved for $I_D$. 

$$I_D = \frac{1}{2} \mu C_{ox} W \left( V_{DD} - I_D R_S - V_{TH} \right)^2$$
Supply-Independent Biasing

If $R_s$ is replaced by a current source, drain current $I_D$ becomes independent of supply voltage.

Example of a CS Stage (I)

$A_v = -g_m \left( \frac{1}{g_{m3}} \parallel r_{01} \parallel r_{02} \parallel r_{03} \right)$

$R_{out} = \frac{1}{g_{m3}} \parallel r_{01} \parallel r_{02} \parallel r_{03}$

$M_1$ acts as the input device and $M_2, M_3$ as the load.
**Example of a CS Stage (II)**

- M1 acts as the input device, M3 as the source resistance, and M2 as the load.

\[
A_v = -\frac{r_{o2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} || r_{o3}}
\]

**Examples of CS and CG Stages**

- With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.

\[
A_{v_{CS}} = -g_{m2}[(1+g_{m1}r_{o1})R_s + r_{o1}] || r_{o1}
\]

\[
A_{v_{CG}} = \frac{r_{o2}}{\frac{1}{g_m} + R_s}
\]
By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.

This example shows that by probing different places in a circuit, different types of output can be obtained.

\[ A_v = \frac{R_D}{1 + \frac{1}{g_{m1}g_{m2}}} \]

\[ \frac{v_{out2}}{v_{in}} = \frac{1}{g_{m3}r_{O3}r_{O4}} \]

\[ \frac{v_{out1}}{v_{in}} = \frac{1}{g_{m2}r_{O2} + \frac{1}{g_{m1}}} \]