<table>
<tr><td rowspan="3"></td><td colspan="4">Course name: EE225 Logic Design Laboratory</td><td colspan="3">Department: Electrical and Electronics Engineering</td><td>Semester</td></tr>
<tr><td></td></tr>
<tr><td colspan="7">Methods of Education</td><td>Credit (ECTS)</td></tr>
<tr><td colspan="8"><table>
<tr><td>Lecture</td><td>Study Time</td><td>Lab</td><td>Homework</td><td>Project</td><td>Exam (incl. Prep.)</td><td>Total</td></tr>
<tr><td>0</td><td>0</td><td>28</td><td>0</td><td>15</td><td>20</td><td>63</td></tr>
</table></td><td>2</td></tr>
<tr><td>Language</td><td colspan="8">English</td></tr>
<tr><td>Compulsory/Elective</td><td colspan="8">Compulsory</td></tr>
<tr><td>Prerequisites</td><td colspan="8">None</td></tr>
<tr><td>Course Contents</td><td colspan="8">Fundamental concepts of Digital Design are mentioned during the semester. Especially, adder, subtracter, multiplexer, encoder and decoder, counter, Flip-Flop design using FPGA using Xilinx ISE platform on BASYS 2.</td></tr>
<tr><td>Course Objective</td><td colspan="8">1. To provide fundamental concepts used in the analysis and design of digital circuits and systems
2. To provide experience to analyze and design of combinational logic circuits
3. To provide experience to experimentally validate combinational logic circuits
4. To provide experience to analyze and design of synchronous sequential circuits
5. To provide experimentally validate synchronous sequential logic circuits
6. To develop skills to work on a project about combinational and/ or synchronous sequential logic circuits
7. To develop skills to prepare effective project report</td></tr>
<tr><td>Learning Outcomes and Competences</td><td colspan="8">Students who pass the course will be able to:
- Perform conversions between number systems, make addition and subtraction in unsigned and complement number systems.
- Analyze and design combinational circuits using tools such as Boolean algebra, Karnaugh map, and etc.
- Analyze and design arithmetic circuits using half adders, subtractors and full adders, subtractors.
- Analyze and design synchronous sequential circuits constructed with flip-flops, shift registers and counters.
- Describe combinational circuits using Verilog hardware description language in structural and behavioral forms.
- Simulate the Verilog code describing combinational logic using simulation software.
- Prepare well written reports.</td></tr>
<tr><td>Textbook and /or References</td><td colspan="8">1. M. Morris Mano, Michael D. Ciletti “Digital Design: With an Introduction to the Verilog HDL ”, Prentice Hall International, 5th Edition, 2012.
2. John F. Wakerly, “Digital Design, Principles and Practices”, Pearson International Edition, 4th Edition, 2007.</td></tr>
<tr><td rowspan="10">Assessment Criteria</td><td colspan="5"></td><td colspan="2">If any, mark as (X)</td><td>Percentage (%)</td></tr>
<tr><td colspan="5">Midterm Exams</td><td colspan="2">X</td><td>20</td></tr>
<tr><td colspan="5">Quizzes</td><td colspan="2">X</td><td>12</td></tr>
<tr><td colspan="5">Homework</td><td colspan="2">X</td><td>3</td></tr>
<tr><td colspan="5">Projects</td><td colspan="2">X</td><td>10</td></tr>
<tr><td colspan="5">Term Paper</td><td colspan="2"></td><td></td></tr>
<tr><td colspan="5">Laboratory work</td><td colspan="2">X</td><td>15</td></tr>
<tr><td colspan="5">Other</td><td colspan="2"></td><td></td></tr>
<tr><td colspan="5">Final Exam</td><td colspan="2">X</td><td>40</td></tr>
<tr><td>Instructors</td><td colspan="8">Assoc. Prof. Enver ÇAVUŞ</td></tr>
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Weekly Schedule	
Week	**Subject**
1	Introduction to the Lab.
2	Setup of Xilinx ISE 14.7
3	Implementation of Gate Level Logic Modules
4	Writing Testbench
5	Modular Implementation of Complex Logic Circuits
6	Generating .ucf file for sending the code to the FPGA card
7	Modular Implementation
8	Minimization of Complex Logic Circuits
9	**Midterm Exam**
10	Clocked Design in Verilog
11	Seven Segment in Verilog
12	Accumulators
13	Arithmetic Logic Unit (ALU) modeling
14	Modeling A Sequence Controller
15	Central Processing Unit (CPU) Modeling